

REMARKS

In these remarks, the Applicant refers by page and line number to both the (1) disclosure as originally filed and the (2) present disclosure, which includes all amendments to date. To maintain clarity, these will be referred to as either the “original disclosure as filed” to indicate the disclosure as originally filed on August 31, 1998, or the “present disclosure” to indicate the present disclosure, which includes all amendments to date.

1. Claim Rejections – 35 USC § 112

Claims 43, 47-54, and 55-66 are rejected under 35 USC § 112, first paragraph, as failing to comply with the written description requirement. The Applicant respectfully traverses the rejection.

The Applicant submits that the original disclosure as filed teaches the subject matter of claim 43. Furthermore, the original disclosure as filed fully supports the “trench-gate” type embodiment of claim 43 even without resorting to material incorporated or expressly included by reference (although referencing such material in support of the claims should not be precluded). The original disclosure as filed also provides full support for similar elements of the “planar-gate” type embodiment by way of express inclusion or incorporation of material by reference (e.g., U.S. Pat. Nos. 4,895,810 and 5,262,336, which were incorporated by reference at page 9, lines 15-17 and page 14, lines 13-14 of the original disclosure as filed).

At page 6 and 7 of the present office action, the Examiner states that the claim(s) contain subject matter which was not described in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. However, the Applicant submits the following evidence which shows possession of the claimed invention at the time the application was filed. Consider that “the vertically-extending source conductor . . . electrically shorting the source region to the active body region across the PN junction” is taught, e.g., at Page 14, Lines 21-25 of the original disclosure as filed. The “gate conductor” is discussed ubiquitously throughout the original disclosure as filed, e.g., at Page 11, Line 18-24, Page 12, Line 8, and Page 13, Line 2. That the gate conductor is comprised of “doped polysilicon” is taught at Page 19, Line 7. Where the gate conductor is “contacting the gate oxide layer within the trench” is recited, e.g., at Page 11, Lines 15-16 and Page 16, Lines 4-8.

A “first metal layer” is taught at Page 11, Line 27 through Page 12, Line 1 of the original disclosure as filed (“A silicide can be formed in the remaining polysilicon material at this step to further reduce gate resistance, for example, by refractory metal deposition and silicide formation.” This identical teaching appears in US 5,283,201 at Column 7, Lines 5-8, a parent of the present application in the lineage of priority benefit claims). That the first metal layer defines “a gate metal layer overlying the doped polysilicon of the gate conductor” is taught, e.g., at Page 11, Line 22 through Page 12, Line 1 of the original disclosure as filed.

Similarly, the remaining elements of claim 43 are likewise taught by the disclosure as originally filed. Claim 43 recites the element of an “insulating layer overlying the gate conductor,” which is taught, e.g., at page 12, Lines 1-3. An “upper metal layer” is taught at Page 14, Lines 20-21 (e.g., “frontside metallization”) and Page 16, Lines 1-4 (e.g., “source metal”). The upper metal layer may have a “first portion contacting the gate conductor through a via in the insulating layer.” This particular feature is originally disclosed at Page 14, Lines 25-28 (“The completion steps also include opening gate contact vias at discrete locations, which can be done in this process without critical alignment, and passivating the surface”). Finally, a “second portion coupled to the source region in electrical isolation from the gate conductor” is taught at Page 16, Lines 1-4. Each claim element is supported by the original disclosure as filed.

Moreover, certain details of exemplary embodiments of the present invention are disclosed in further particularity in related applications (e.g., U.S. Pat. Nos. 4,895,810 and 5,262,336), which—as previously noted—were incorporated by reference at page 9, lines 15-17 and page 14, lines 13-14 of the original disclosure as filed. In subsequent amendments, the Applicant expressly included selected teachings into the present disclosure. As set forth in the MPEP, “[t]he information incorporated is as much a part of the application as filed as if the text was repeated in the application, and should be treated as part of the text of the application as filed. Replacing the identified material incorporated by reference with the actual text is not new matter.” MPEP §2163.07(b). Such amendments were made to expressly recite certain language and figures of previously incorporated material and, therefore, no new matter was introduced.

Furthermore, the expressly recited portions—and other matter incorporated by reference—demonstrate support of the claimed subject matter at least for the purpose of conveying to one skilled in the relevant art that the Applicant, at the time the application was filed, had possession of the claimed invention. As explained above, full support for the

“trench-gate” type embodiment of claim 43 is found in the original disclosure as filed even without resort to the material incorporated or expressly included by reference (although, as the Applicant notes, referencing such material in support of the claims should not be precluded). And full support for similar elements of the “planar-gate” type embodiment is given by the present disclosure by way of express inclusion or incorporation of material by reference.

Additionally, a metallization layer (“first metal layer”) overlying doped polysilicon of a gate is taught in the context of a “planar-gate” type embodiment at Column 11, Lines 60-68 of U.S. 5,262,336. Similarly, the first metal layer is taught in the context of a “trench-gate” type embodiment at Page 11, Lines 27 through Page 12, Line 1 of the original disclosure as filed—without resort to the material incorporated by reference. Such metallization serves to reduce gate resistance (Original Disclosure as filed, Page 11, Lines 27-28) and reduces signal propagation delay (US 5,262,336, Column 15, Lines 36-38). Further to this teaching, US 5,262,336 makes clear that the metal layer may be aluminum (Column 11, Lines 61-63) or a refractory metal such as tungsten or metal-silicide (Column 24, Lines 18-20). The metal layer can be provided by a number of techniques including cold evaporation or sputtering (Column 23, Lines 67-68), selective vapor deposition (Column 24, Line 20), or electroplating (Column 24, Lines 20-21).

In other words, there is no meaningful distinction between metallizing an exposed surface of doped polysilicon in a “planar-gate” type embodiment vis-à-vis a “trench-gate” type embodiment. Both instances teach a metallization atop the polysilicon surface and an insulative layer applied over the metal layer (US 5,262,336, Column 24, Lines 32-40 and Lines 59-60, and Original Disclosure as filed, Page 12, Lines 1-3). In due course, an “upper metal layer” is deposited in both instances (as taught in US 5,262,336 Column 15, Lines 8-14 and Lines 51-54 for the “planar-gate” type embodiment—also as taught in the original disclosure as filed at Page 14, Lines 20-21 and Page 16, Lines 1-4 for “trench-gate” type embodiment). Regardless of distinctions between the “trench-gate” and “planar-gate” type embodiments, metallization of the gate polysilicon is supported by the original disclosure as filed without resort to any incorporated matter (as in the case of the “trench-gate” embodiment), as well as by incorporated matter (as in the case of the “planar-gate” embodiment).

The Examiner suggests that the disclosure lacks an adequate description regarding how and/or where such “planar-type” contact structures could be applied to the “trench-gate”

type structures given that the gate contact (62 in Fig. 12) in the active region is already formed and fully surrounded by insulating layers (60, 48, and 68) during the formation of the source contact (94). However, the original disclosure as filed explicitly describes how, when, and where the gate metallization is applied prior to the insulating layer 68. "A silicide can be formed in the remaining polysilicon material at this step to further reduce gate resistance, for example, by refractory metal deposition and silicide formation. Then, a CVD oxide (or oxynitride) isolation layer 68 is deposited into the trenches 50 over the remaining polysilicon material 64 and over the trenching protective structures 40." (Page 11, Line 27 through Page 12, Line 3 of the original disclosure as filed). Second layer metal contact to gate conductor is given on Page 14, Lines 26-27 as part of the front metal formation of layer 94. A person having ordinary skill in the art would be fully informed by the original disclosure as filed alone that the elements of claim 43 were in possession of the Applicant at the time of filing. Furthermore, other features set forth in the disclosures which are incorporated by reference provide added support for deposition of various metals atop the exposed polysilicon gate surface before insulative deposition (e.g., US 5,262,336, Column 24, Lines 32-40 and 59-60). Thus, the Applicant submits that claim 43 is in proper form for allowance.

The Examiner also rejects claims 47-54 and 55-66 as failing to comply with the written description requirement of 35 USC § 112, but did not specify in which respects these claims fail to comply. The Applicant respectfully traverses the rejection. Claims 47-48, 54, and 58 correspond directly to original claims 22, 23, 29, and 32, respectively, as originally filed. As such, these original claims are part of establishing an original disclosure (see MPEP 608.01(I)). Remaining claims 49-53, 55-57, and 59-66 are supported either by the original disclosure as filed, including originally filed claims, or by the disclosures which are incorporated by reference.

For example, the following claims are supported by at least the original disclosure as filed: claim 49 is supported by at least original claim 24 and Page 14, Lines 10-14; claim 50 is supported by at least original claim 25 and Page 15, Line 26 to Page 16, Line 2, and Page 14, Lines 4-6; claim 51 is supported by at least original claim 26 and Page 10, Lines 22-27; claim 52 is supported by at least original claim 21, Page 14, Lines 20-25, and Page 15, Line 23 to Page 16, Line 8; claim 53 is supported by at least original claim 28 and Page 14, Lines 20-25; claim 55 is supported by at least original claim 30, Page 15, Lines 8-22, and Page 10, Lines 16-17; claim 56 is supported by at least original claim 30, Page 10, Lines 14-15, and Page 11, Lines 13-14; claim 57 is supported by at least original claim 31 and Page 7, Lines

14-16; and claim 59 is supported by at least original claim 33 and Page 18, line 24 to Page 19, Line 7.

Similarly, the following claims are supported by at least US 5,262,336: claim 60 is supported by at least Column 11, Lines 61-63; claim 61 is supported by at least Column 24, Lines 20-21; claim 62 is supported by at least Column 24, Lines 18-20; claim 63 is supported by at least Column 24, Lines 20-21; claim 64 is supported by at least Column 11, Lines 61-63; claim 65 is supported by at least Column 11, Lines 61-63 and Column 15, Lines 8-14; and claim 66 is supported by at least Column 24, Line 61 through Column 27, Line 50.

Thus, based at least on the original claims of the original disclosure, the original disclosure as filed, and the disclosures incorporated by reference, claims 47-54 and 55-66 are supported and should also be allowable.

2. Objection to Drawings under 37 CFR 1.83(a)

The Examiner objects to the drawings and states that the subject matter recited in claim 43 must be shown or the feature(s) canceled from the claims. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). No new matter should be entered.

The Applicant submits new figure Fig. 7A, labeled "NEW SHEET," which illustrates a first metal layer 230 overlying doped polysilicon 62. The Applicant submits new figure Fig. 13A, labeled "NEW SHEET," which illustrates frontside metal delineating gate and source electrodes 94 and gate contact via 97. The Applicant also resubmits herewith prior Fig. 6B and 6C with the requested marking "REPLACEMENT SHEET." No new matter is entered.

The Applicant notes that "information contained in any one of the specification, claims or drawings of the application as filed may be added to any other part of the application without introducing new matter." MPEP 2163.06 Relationship of Written Description Requirement to New Matter. Support for Fig. 7A is originally disclosed at Page 11, Line 27 through Page 12, Line 1 ("A silicide can be formed in the remaining polysilicon material at this step to further reduce gate resistance, for example, by refractory metal deposition and silicide formation"). As such, the Applicant submits Fig. 7A, which is a copy of original Fig. 7 with the metal layer 230 on the surface of the polysilicon material 62, as shown. Support for Fig. 13A is originally disclosed at Page 5, Lines 10-11 ("Frontside metal

is deposited and patterned to delineate the gate and source (cathode) electrodes”) and at Page 14, Lines 25-28 (“The completion steps also include opening gate contact vias at discrete locations, which can be done in this process without critical alignment, and passivating the surface”). As such, the Applicant submits Fig. 13A, which generally corresponds to Fig. 13, with the addition of gate contact via 97, as shown.

The Applicant provides the following annotated excerpt of claim 43 to show that every element is present in the original disclosure of the present application, and shown in the drawings:

“a vertically-extending source conductor 96 contacting the vertically-oriented layer 86/90 on a side thereof opposite the gate oxide layer 60 and gate conductor 62, the source conductor 96 electrically shorting the source region 86 to the active body region 90 across the PN junction; the gate conductor 62 comprising doped polysilicon 62 contacting the gate oxide layer 60 within the trench 70 and a first metal layer 230 defining a gate metal layer 230 overlying the doped polysilicon 62 of the gate conductor 62; an insulating layer 68 overlying the gate conductor 62; and an upper metal layer 94 over the insulating layer 68 and having a first portion contacting the gate conductor through a via 97 in the insulating layer 68 and a second portion 96 coupled to the source region 86 in electrical isolation from the gate conductor 62.”

As demonstrated above, each element of claim 43 is shown in the drawings of the present application, including new figure Figs. 7A and 13A, and described in the specification.

The Examiner also suggests that “many of the reference characters shown in Figs. 16B and 16C are not mentioned in the specification.” OA, Page 4. It is unclear which figures the Examiner is referring to because the present application does not have a Fig. 16B or 16C. To the best of the Applicant’s understanding, the Examiner is referring to Figs. 6B and 6C. However, the Applicant is still unclear as to this objection because every reference character for these figures is mentioned in the previous amendment by way of express recitation of language from patents which were originally incorporated by reference, with the only difference being that the reference character numbers were updated to match the present disclosure.

To demonstrate, in the context of Fig. 6B, reference characters 275, 276, 232, 262a, and 263 are mentioned at page 12, Lines 9-16 of the present disclosure. Remaining reference characters 218, 220, 222, 224, 224a, 226, 240 of Fig. 6B are mentioned at Page 12, Line 27

through Page 13, Line 6 of the present disclosure. And in the context of Fig. 6C, reference characters 228, 230, 272, and 274 are mentioned at Page 16, Lines 11-25 of the present disclosure. Remaining characters 218, 219, 220, 222, 224, 225, 226, 232, 262, 264, and 271 of Fig. 6C are mentioned at Page 17, Lines 3-12 of the present disclosure.

Thus, the Applicant submits that all figures, including new Figs. 7A and 13A, show every feature specified in the claims in accordance with 37 CFR 1.83(a). Furthermore, the reference characters of Figs. 6B, 6C, and 7A are also mentioned in the present disclosure. As a result, the Applicant respectfully requests that the Examiner remove any objection to the drawings.

3. New Matter under 35 USC 132(a)

The Examiner suggests that an amendment made on 12/4/2001 with respect to three paragraphs starting with “Further to the completion . . .” constitutes new matter such that full support for such subject matter is not found in the original disclosure or in any of the original disclosure of its parent applications, including the ones of US Patents 4,895,810 and/or 5,262,336. The Applicant respectfully traverses the rejection.

The Applicant submits that the three paragraphs indicated by the Examiner do not introduce new matter into the disclosure. “Replacing the identified material incorporated by reference with the actual text is not new matter.” MPEP §2163.07(b). The language included in the three paragraphs is substantively supported by US 5,262,366 as follows:

With respect to the first paragraph, “a second layer of metal is deposited in gate pad regions of the gate contact layer in isolation from the source pads over a passivation layer” (Column 15, Lines 51-54); “a double or a triple layer of metal can be deposited in the source bonding pad and bus areas” (Column 15, Lines 40-42); and “this measure improves current handling capability, links the source metal areas together in isolation from the gate pads and busses” (Column 15, 42-44).

With respect to the second paragraph, “a layer 272 can be applied on top of areas 230 and 228. This layer may be a resin such as photoresist or any number of other compounds such as polyimide or spin-on glass” (Column 24, Lines 32-35); “layer 272 is applied to assist surface planarization and may be applied using spin, spray, or roll-on techniques familiar to one skilled in the art to give the preferred coating” (Column 24, Lines 35-40); “planarization can be done by conventional techniques familiar to one skilled in the art, such as plasma etching, ion milling, reactive ion etching, or wet chemical etching” (Column 24, Lines 43-

46); “the underlying layers 228 and 230, of the source and gate respectively, remain covered and thus unetched” (Column 24, Lines 46-47); “next, artifacts 274 are etched away, and any metal extending downward along the sidewalls can be removed by continuing the etch” (Column 24, Lines 52-55); “in some procedures, layer 272 is then removed by any conventional means. However, if layer 272 is a material that can remain on the device surface, such as glass, its removal is not necessary” (Column 24, Lines 57-60); and “a passivation layer is then deposited, as is commonly done” (Column 24, Lines 65-66).

And finally, with respect to the third paragraph, “the passivation layer comprises at least one of the group consisting of oxide, nitride, glass and phosphosilicate glass (PSG)” (Column 24, Lines 61 through Column 27, Line 50).

At page 6 of the present office action, the Examiner further suggests that the “planar-type” contact structures are not directly applicable to the “trench-gate” structures, given that the gate contact (62 in Fig. 12) in the active region is fully surrounded by insulating layers (60, 48, and 68) during the formation of the source contact (94). However, the original disclosure as filed—even without resorting to material incorporated by reference—teaches the deposition of a metal contact layer on the gate polysilicon prior to depositing insulating layer 68. As a result, the gate contact is not fully surrounded by insulating layers during the formation of the first metal layer (layer 230 as shown in FIG. 7A, and taught at Page 11, Line 27 through Page 12, Line 3 of the original disclosure as filed). To reiterate, applying a first metal layer to polysilicon prior to applying an insulating layer is a teaching supported both in the original disclosure as filed with respect to “trench-gate” type embodiments, as well as in the incorporated-by-reference disclosures with respect to “planar-gate” type embodiments. The Applicant submits that such contact structures are directly applicable to both the “trench-gate” and “planar-gate” type embodiments. Thus, the Applicant respectfully requests that the Examiner remove any objection based on new matter.

4. Election / Restrictions

The Examiner suggests that claims 98-101 and 103, which were added in the 5/23/2001 amendment further amended in the 11/3/2006 amendment, are directed to an invention that is independent or distinct from the invention originally claimed. The Examiner has constructively elected by original presentation for prosecution on the merits, and withdraws the claims from consideration as being directed to a non-elected invention.

37 CFR 1.142(b) and MPEP § 821.03. The Applicant acknowledges the Examiner's constructive election without traverse.

In view of the foregoing amendments and remarks, the application should now be allowable. If there are any questions, the Examiner is requested to call the undersigned.

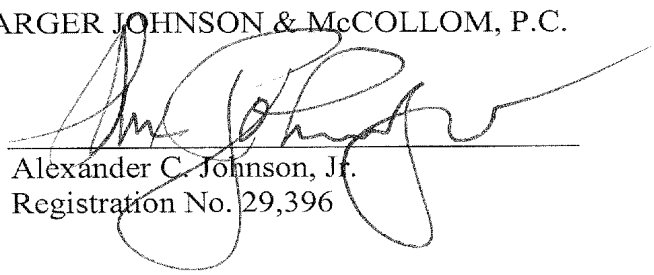
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